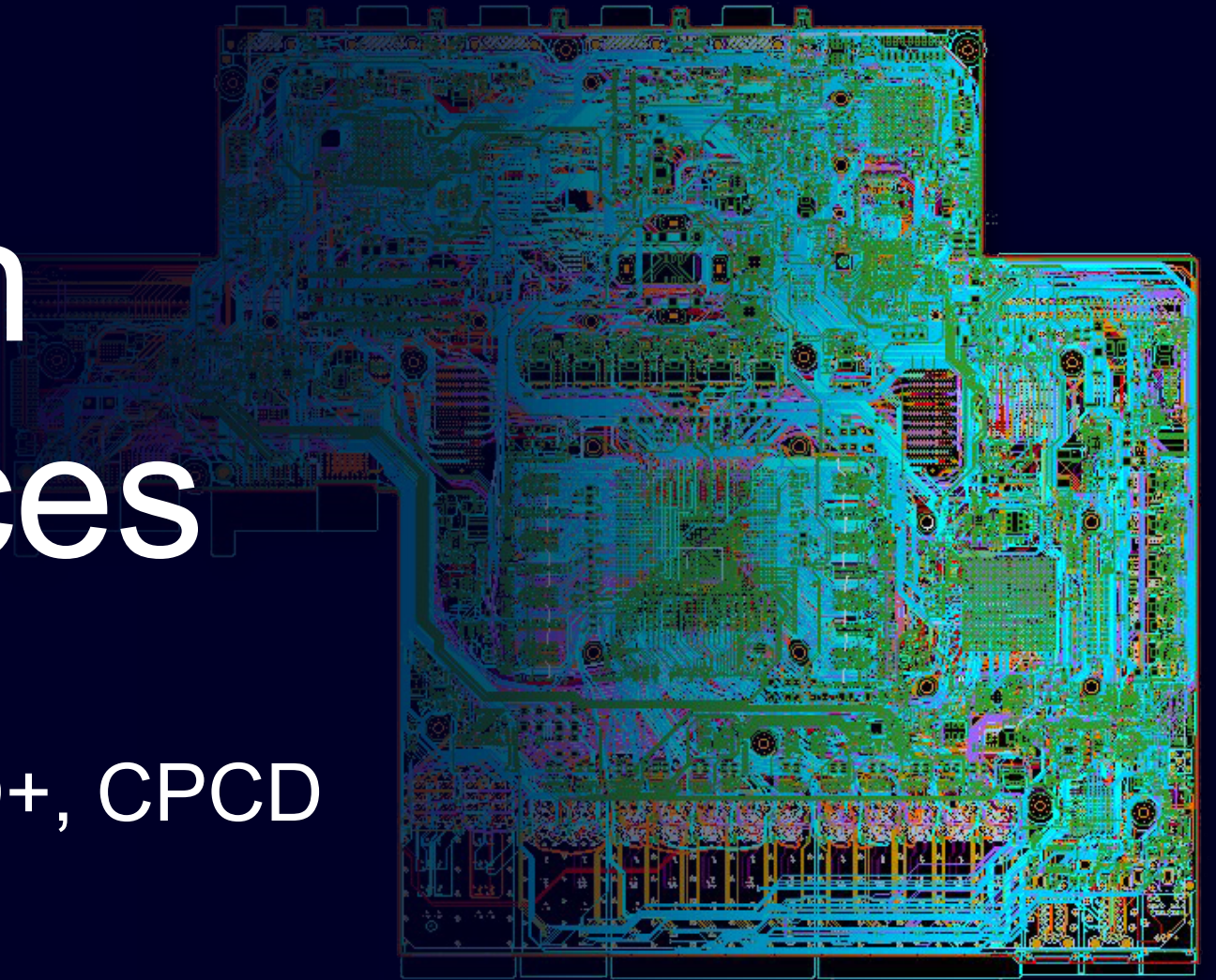
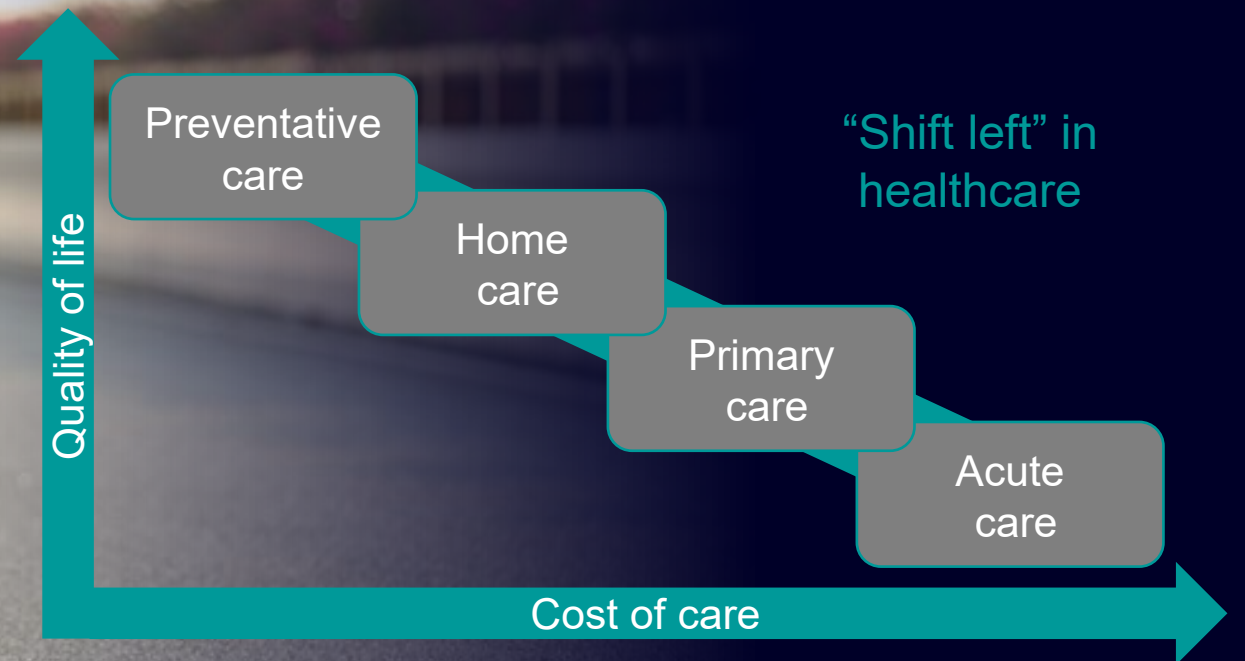


PCB Design Best Practices

Stephen V. Chavez, MIT, CID+, CPCD



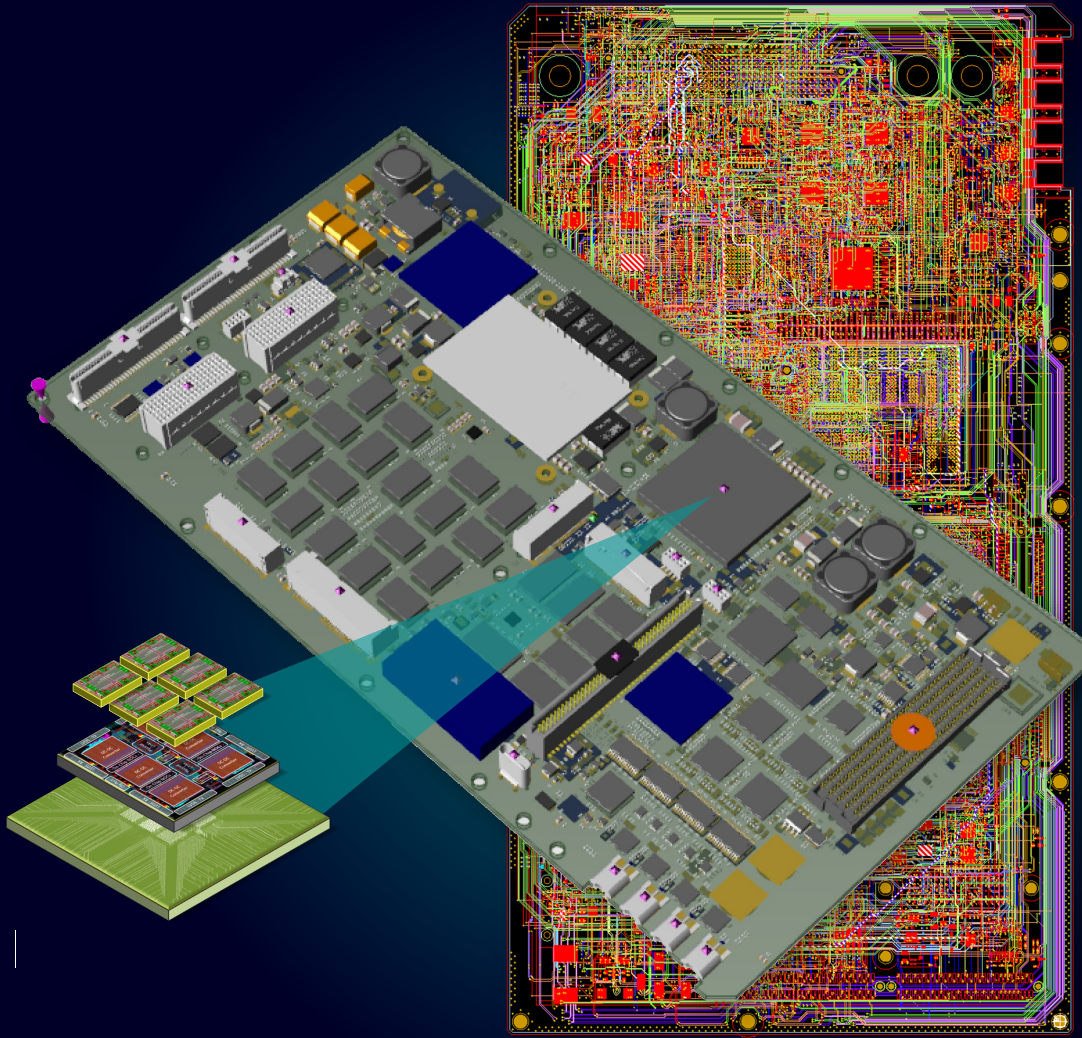
Investment up front pays off in the long term



The state of design in electronics

Design teams **must deliver more complex products** on **even more compressed schedules**, but they **lose valuable time** with unproductive tasks. **Connect them** through all engineering disciplines and give them **best-in-class solutions** to thrive with a **collaborative** approach to **Electronic Systems Design**.

Challenges in PCB Systems Design



Product Complexity

Advanced packaging technologies · Transmission speeds · Multi-discipline co-design · Component count & density · Form-factor · Material technologies

Organizational Complexity

Collaboration across engineering disciplines · Collaboration across geographies · Knowledge management · Workforce productivity & efficiency

Process Complexity

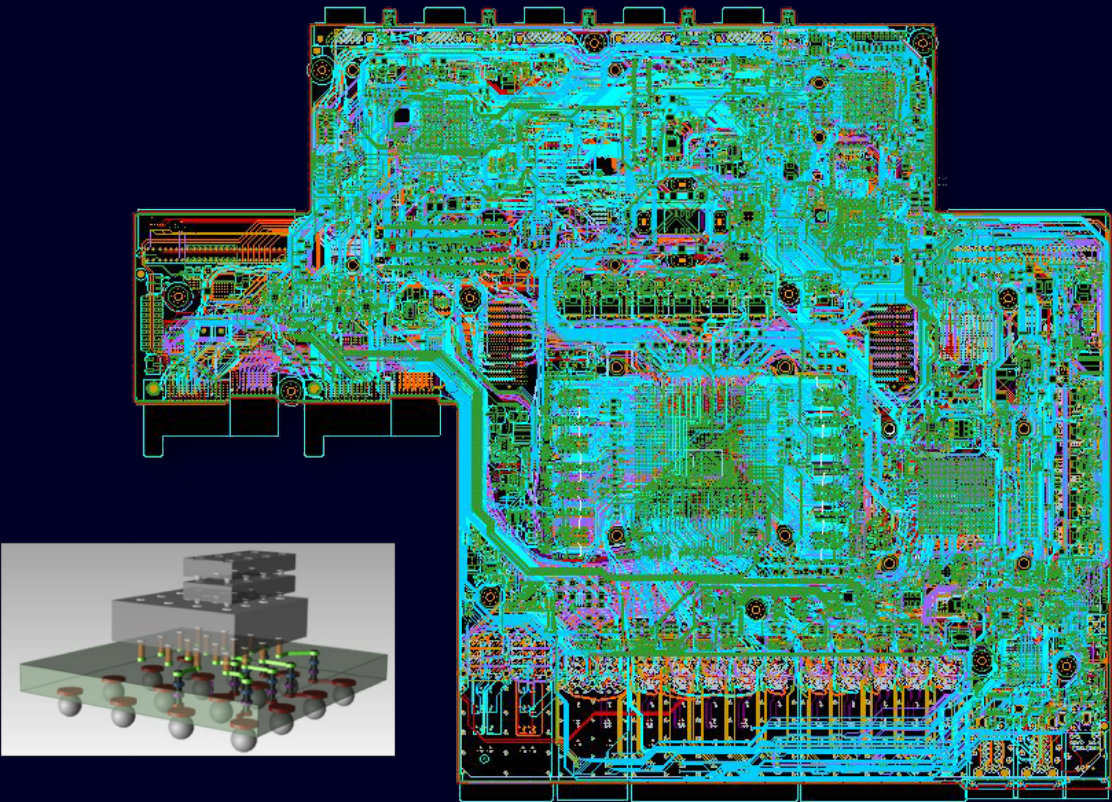
User-experience · Integrated verification · Heterogenous tool chain · System engineering · System decomposition & verification · Streamline design to manufacturing

Supply Chain Complexity

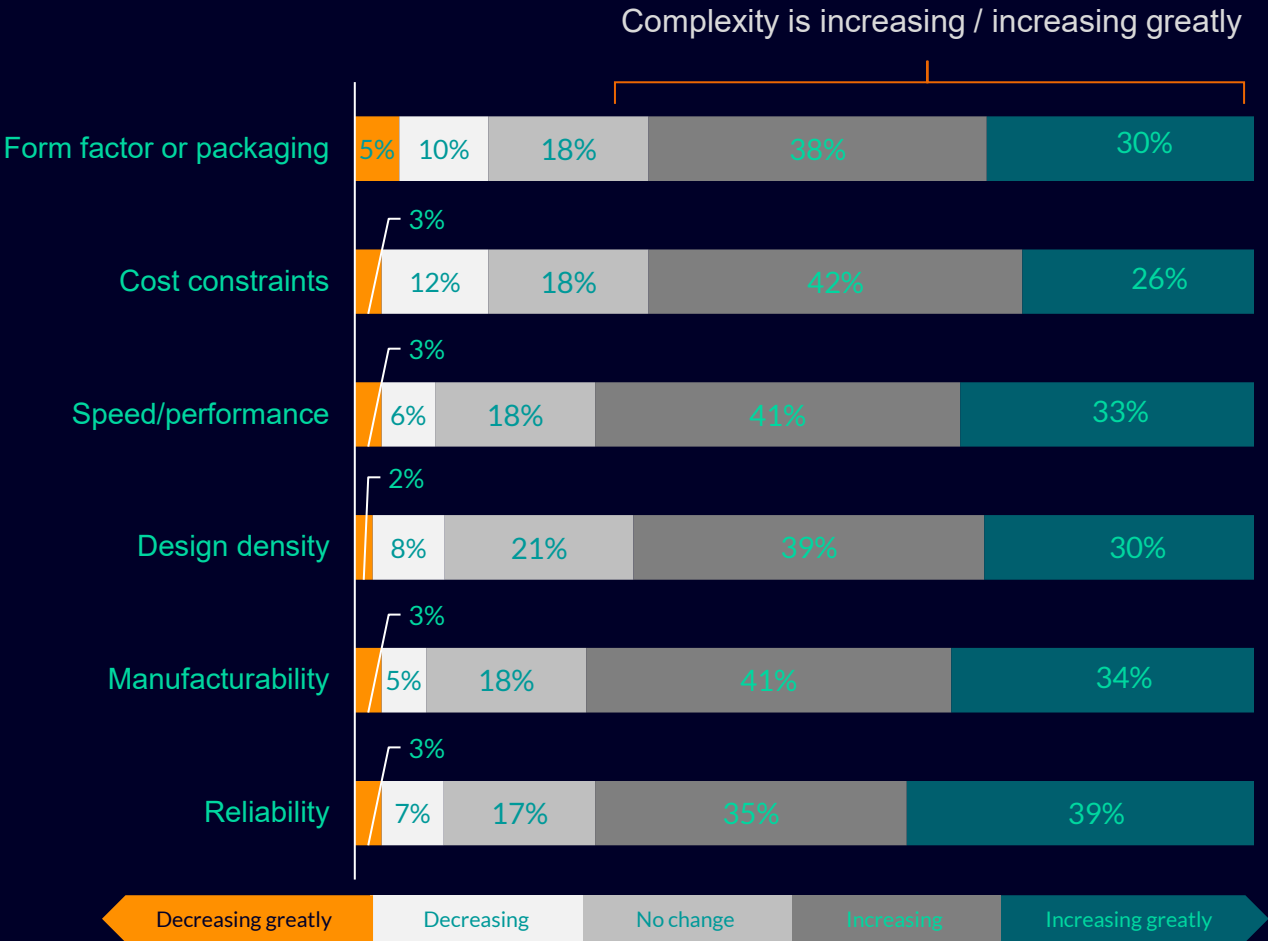
Global supply shortages · Contractor management & assessment · Alternate supply · Pricing volatility · Risk assessment · Sourcing visibility & knowledge

Product Complexity

Advanced packaging technologies · Transmission speeds · Multi-discipline co-design · Component count & density · Form-factor · Material technologies



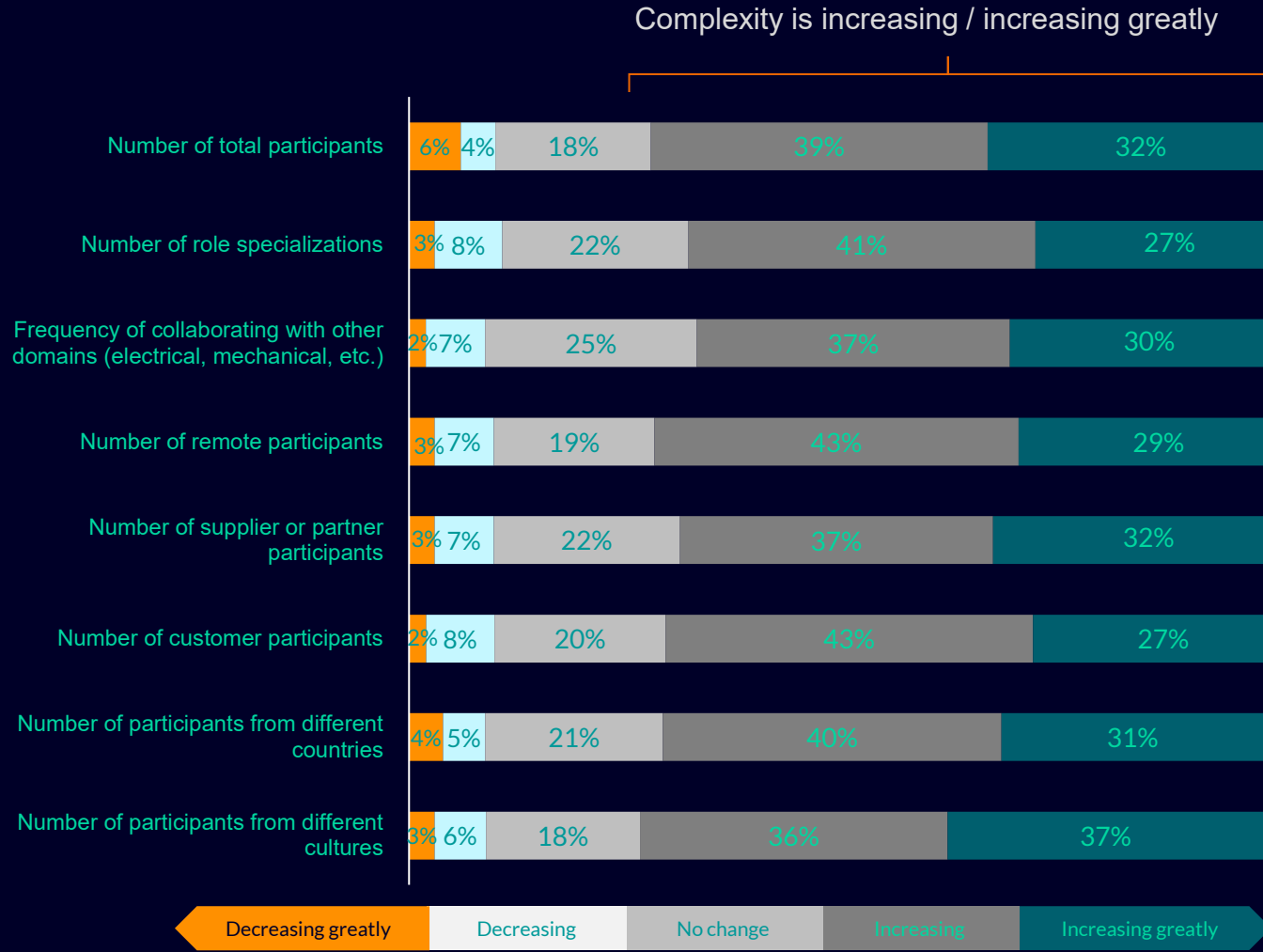
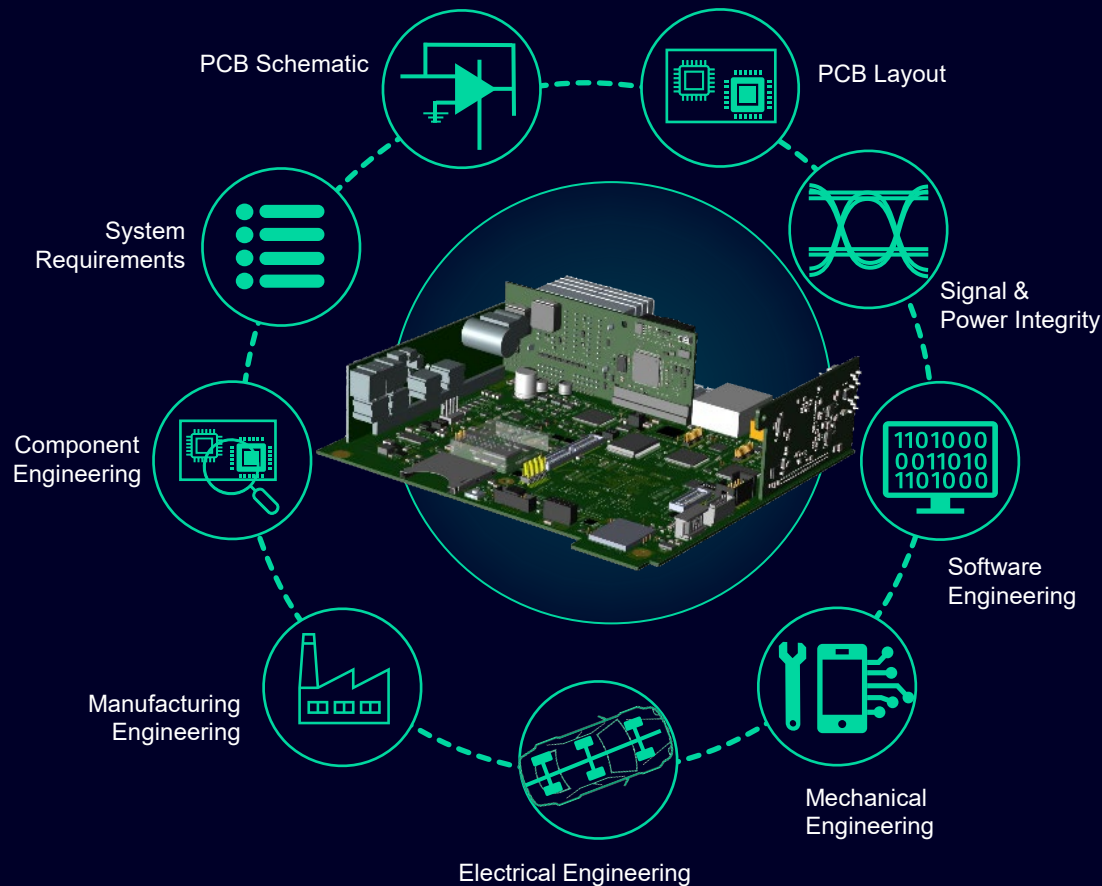
Infinera, 2020 Technology Leadership Awards



Lifecycle Insights, September 2021

Organizational Complexity

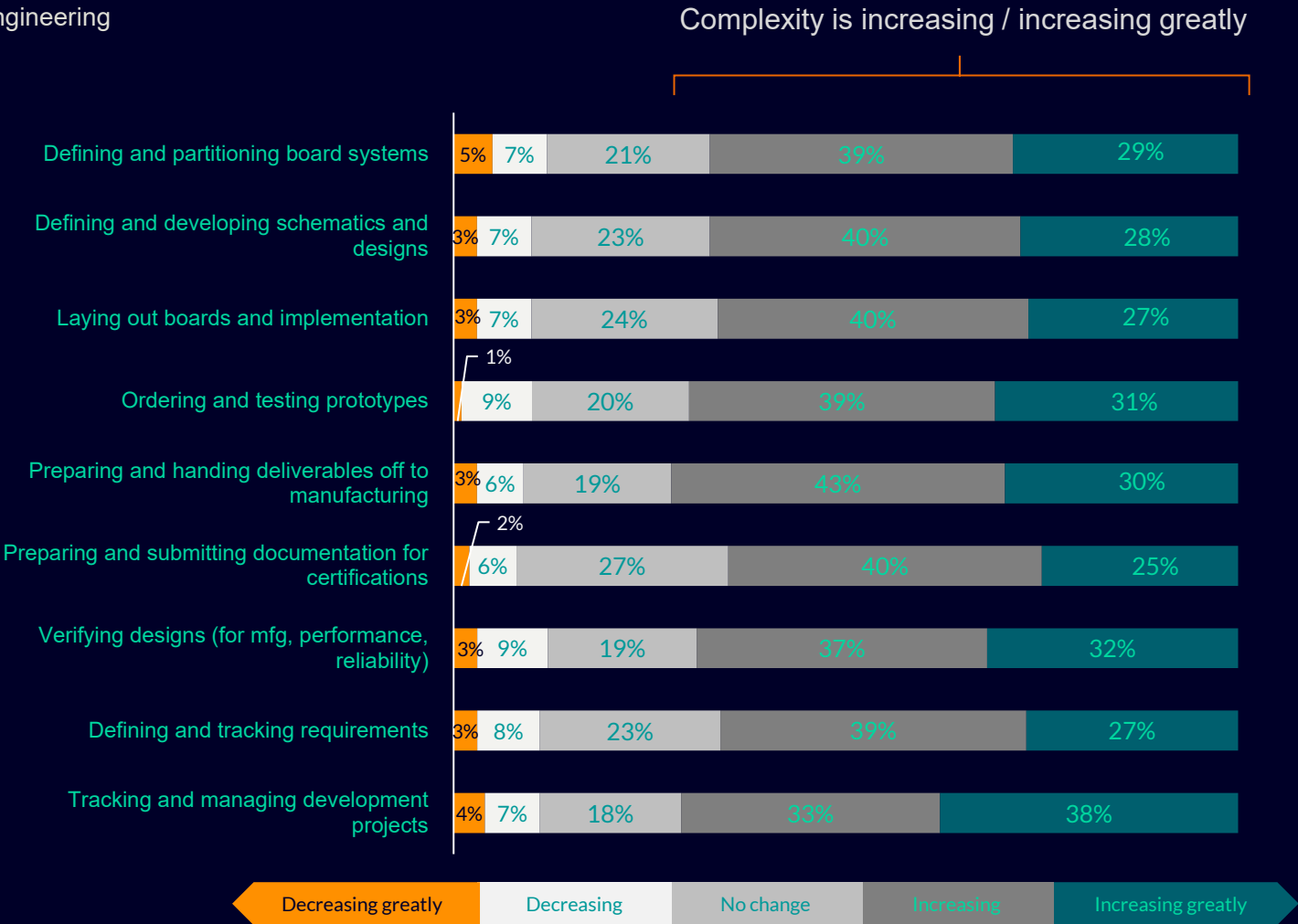
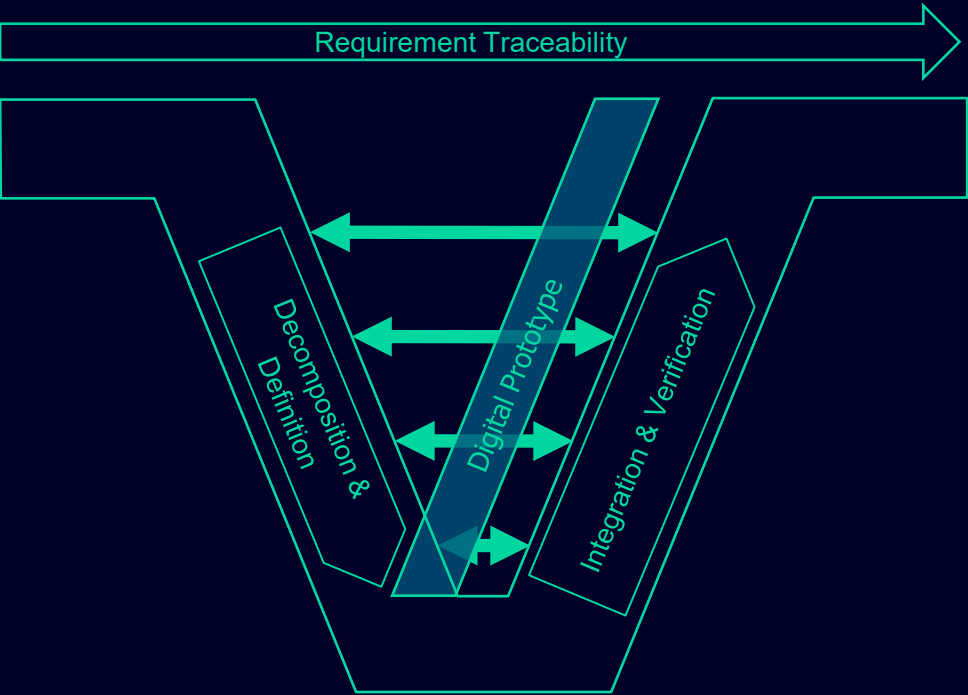
Collaboration across engineering disciplines · Collaboration across geographies · Knowledge management · Workforce productivity & efficiency



Lifecycle Insights, September 2021

Process Complexity

User-experience · Integrated verification · Heterogenous tool chain · System engineering
· System decomposition & verification · Streamline design to manufacturing



Lifecycle Insights, September 2021

Supply Chain Complexity

Global supply shortages · Contractor management & assessment · Alternate supply · Pricing volatility · Risk assessment · Sourcing visibility & knowledge



91%

Indicate sourcing issues have caused product launch delays

81%

Report commodity availability has forced expensive spot buys

79%

Say collaboration issues have caused delays in new product introductions

63%

Express the number of indented levels of a BOM have increased significantly

Sources: Dimensional Research, State of Electronics Sourcing: A Survey of Sourcing Decision-Makers, 2020
Lifecycle Insights, NPI and Sourcing Study, 2021

Best Practices

Definition per Merriam-Webster

A procedure that has been shown by research and experience to produce optimal results and that is established or proposed as a standard suitable for widespread adoption

What are they!

- Best practices are standards or guidelines that are known to produce good outcomes if followed
-

Best Practice Benefits

- Optimized processes and team collaboration
- Reduced design time, respins and eng. costs
- Faster time to market
- Increased reliability and quality of designs



Common Reasons for Status Quo in PCB Design

Problem!

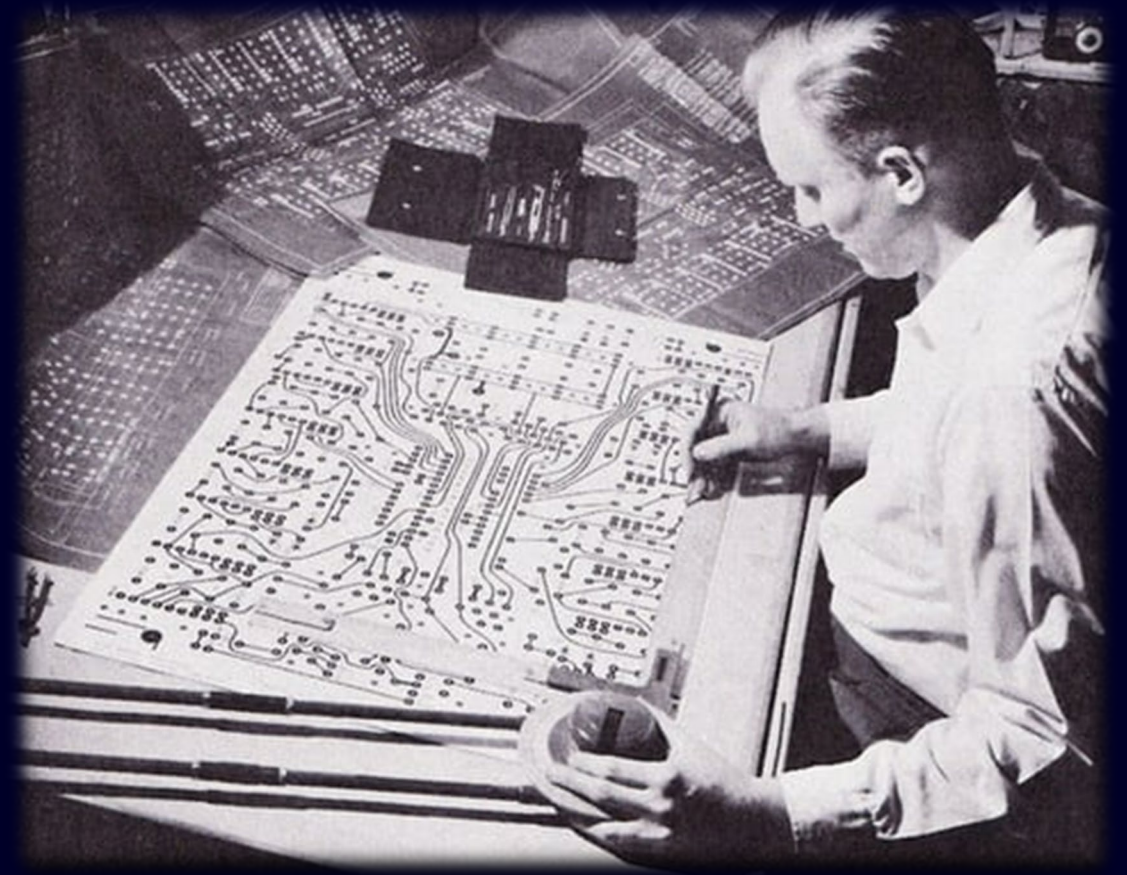
“Always did it that way”

Roadblocks!

- Current process ‘works’ (a manual approach)
- Don’t trust today’s EDA tools
- Internal company culture resistance to change
- No time to learn or train on new functions in tool

Best Practice

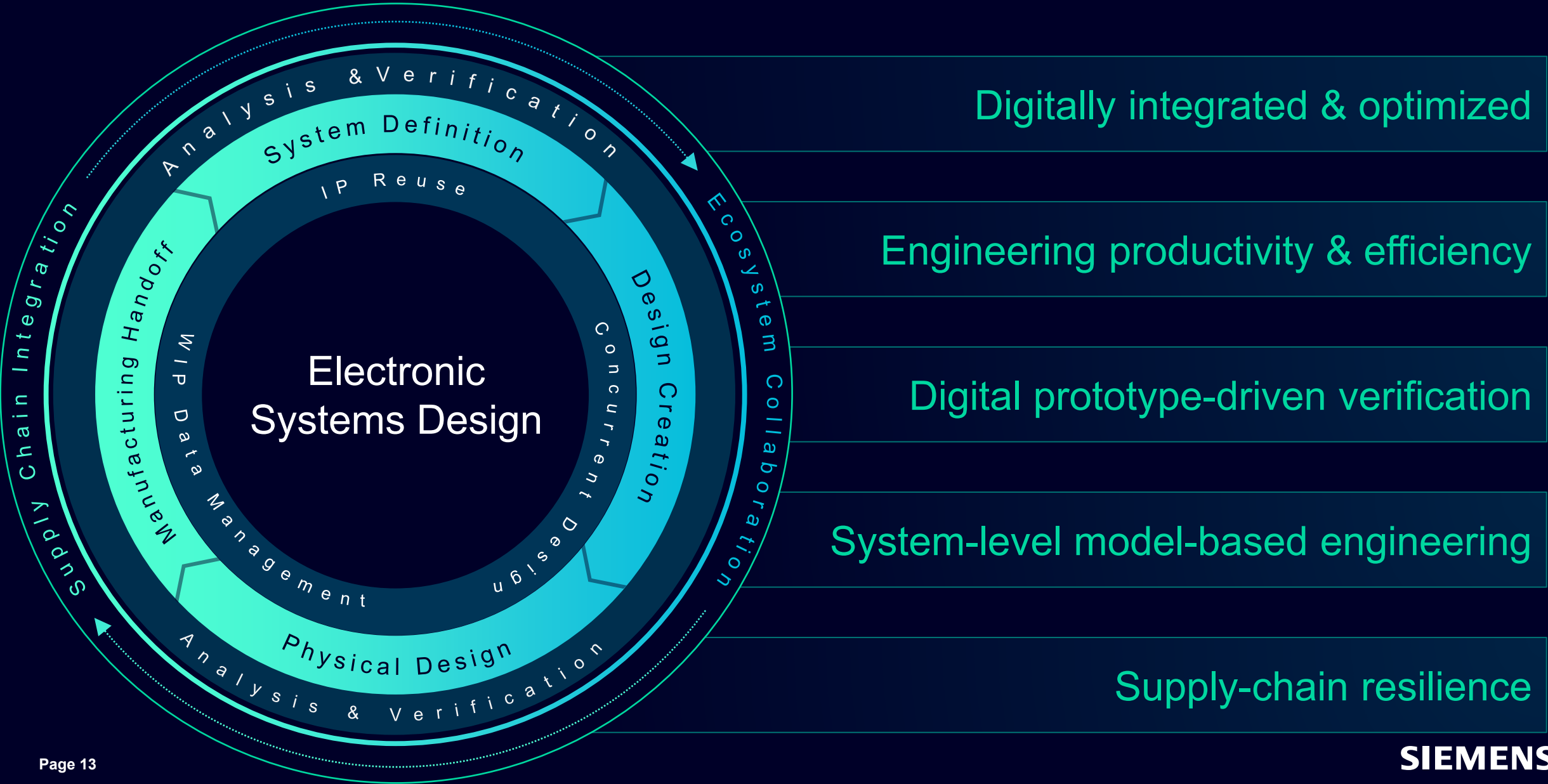
- Constantly seek to optimize internal processes
- Keep up-to-date with today’s EDA tool capabilities and functionalities



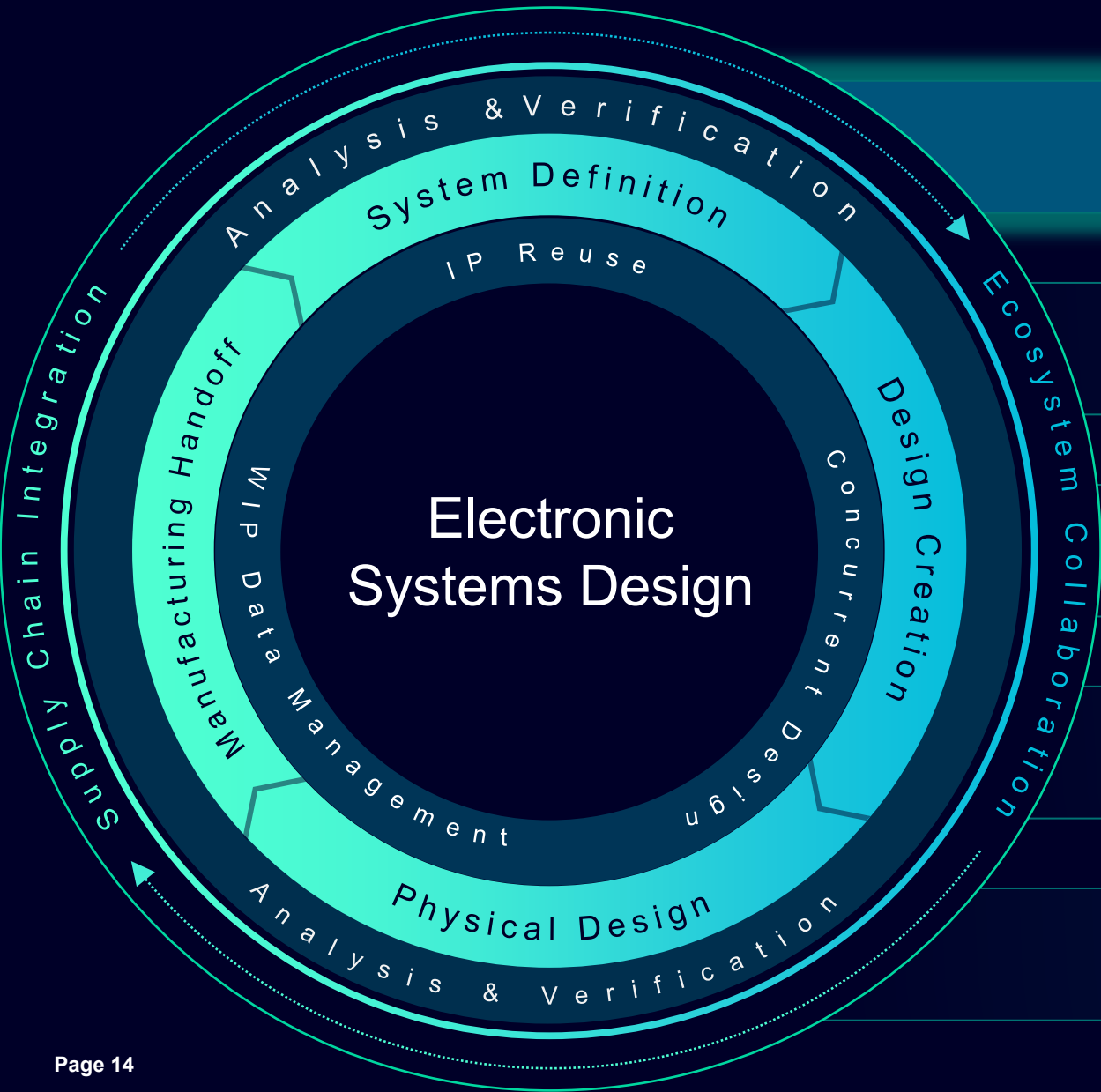
Drawing a PCB with tape and mylar before EDA arrived

Image from *A Manual of Engineering Drawing for Students and Draftsmen, 9th Ed.*, by French & Vierck, 1960, p. 487.

Pillars of Best Practices



Pillars of Best Practices



Digitally integrated & optimized

Engineering productivity & efficiency

Digital prototype-driven verification

System-level model-based engineering

Supply-chain resilience

Electronic-Mechanical Co-design

Problem!

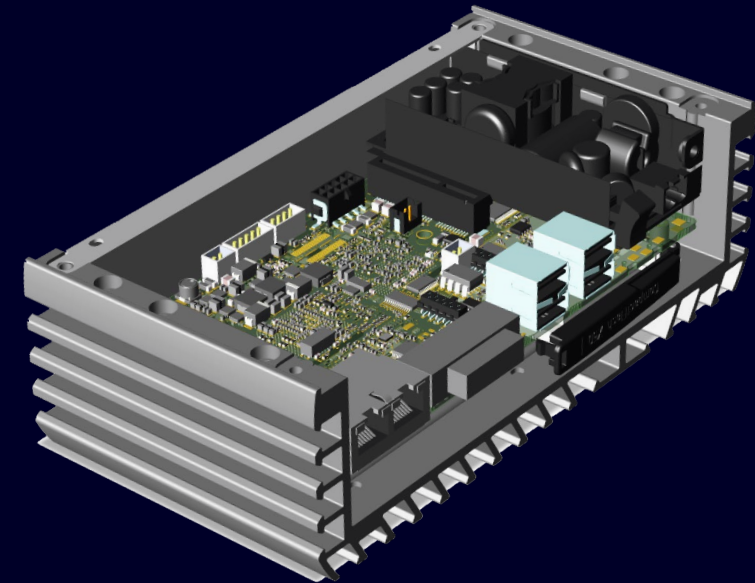
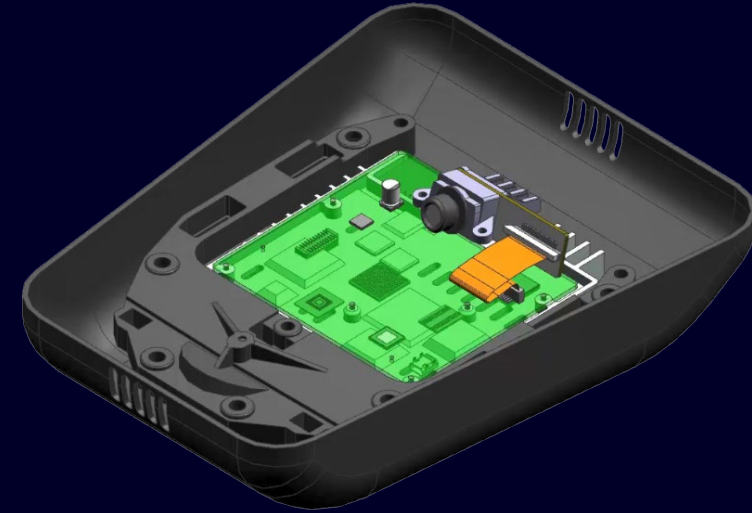
Error prone and inefficient process

Roadblocks!

- Organizational resistance to change
- Siloed teams and independent toolsets
- Unfamiliar with latest format standards

Best Practice

- Adopt latest exchange formats (IDX)
- Look at methodologies that enables context-based, incremental collaboration between domains



Design / Manufacturing

Problem!

Data not addressing producibility or manufacturability passed to manufacturing

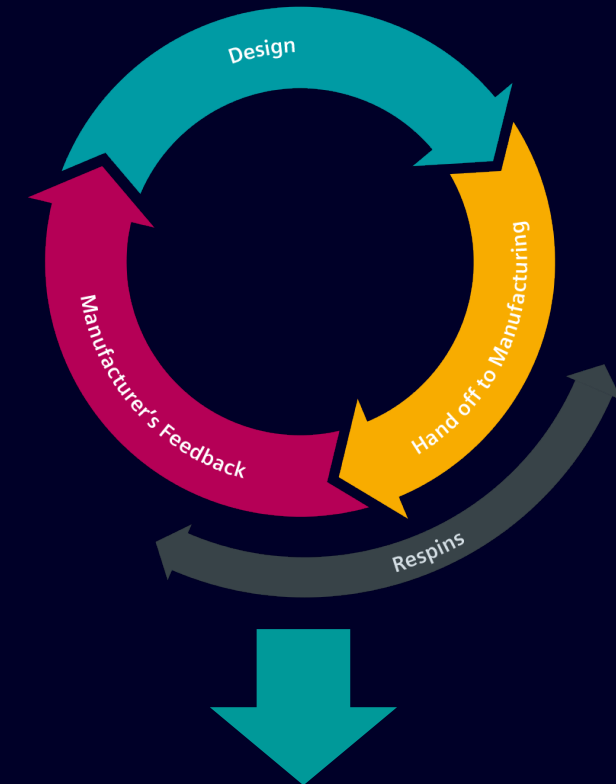
Roadblocks/Inhibitors!

- Competitive pressure on Fab house to accept poor data
- No time to run DFM analysis

Best Practice

- Optimize integration between design and MFG
- Enable lessons learned in MFG to influence designs (enable feedback loop)
- Utilize intelligent data format (ODB++, IPC-2581)

Traditional iterative design flow



Concurrent DFM



Library and Data Management

Problem!

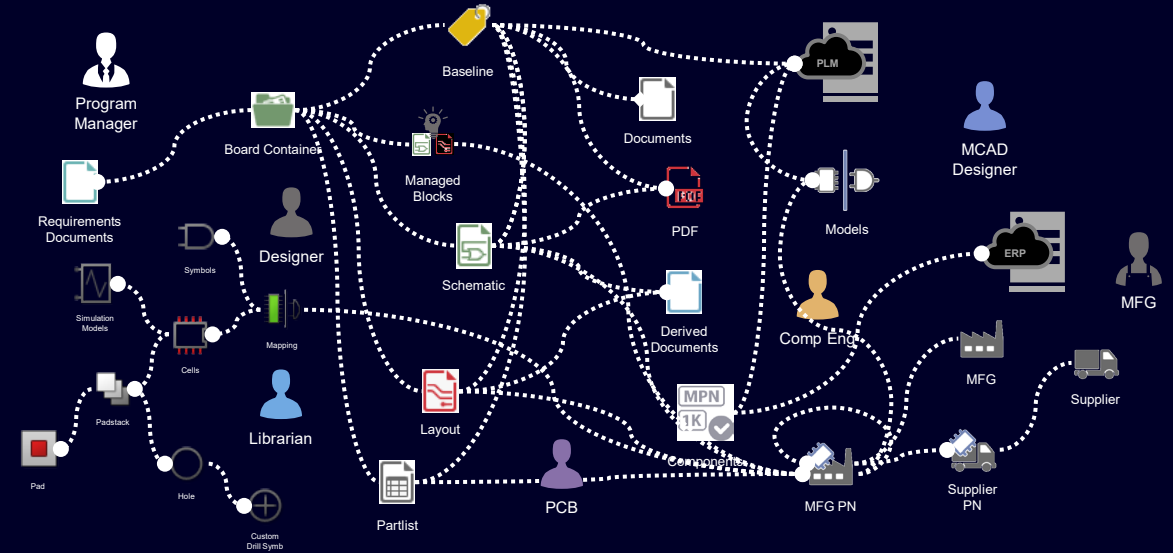
Ineffective collaboration across teams

Roadblocks!

- Product/organizational/process complexities
- Too much overhead to maintain
- No experience/specialist

Best Practice

- Establish internal guidelines & processes
- Utilize industry standards
- Organize and control your library and data



Work-in-progress Design Management

Problems!

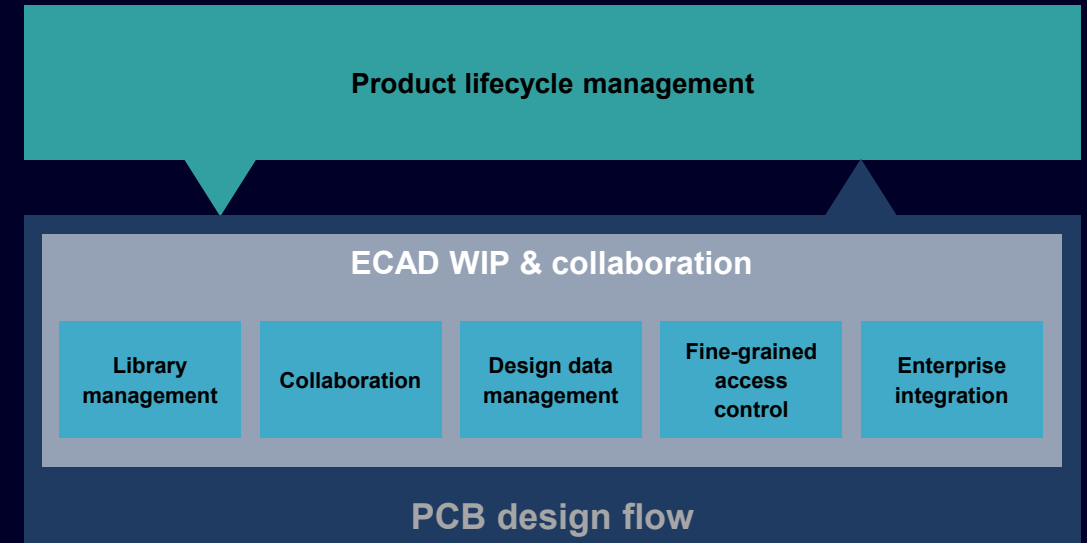
In-process status visibility not adequately shared across functions

Roadblocks!

- Home grown manual processes in place
- Too much overhead to maintain / complexities
- Unaware of opportunities to be better optimized

Best Practice

- Deliver instant status updates and visibility
- Facilitate team integration & optimization
- Attack multi-domain roadblocks instantly and on the fly



PLM Integration

Problem!

Lacking product management and tool integration

Roadblocks!

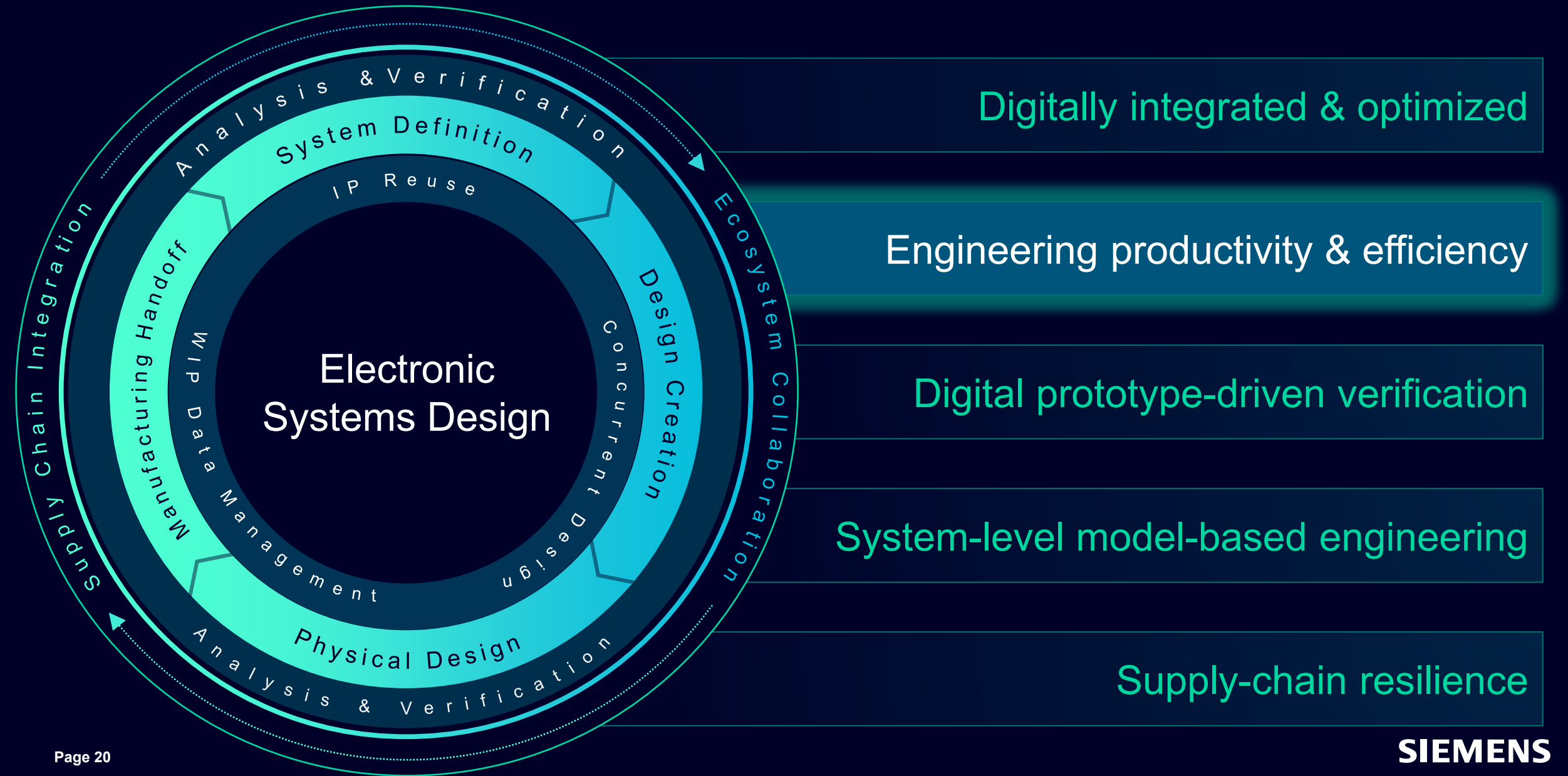
- Local server or computer is used as data hub
- Too much overhead to maintain, access issues
- No experience/specialist

Best Practice

- Provide superior control and tracking of product data with:
 - Master version of the truth
 - Where-used / traceability / status / approvals
 - Data security / archiving



Pillars of Best Practices



Automation – Placement, Route, Outputs

Problem!

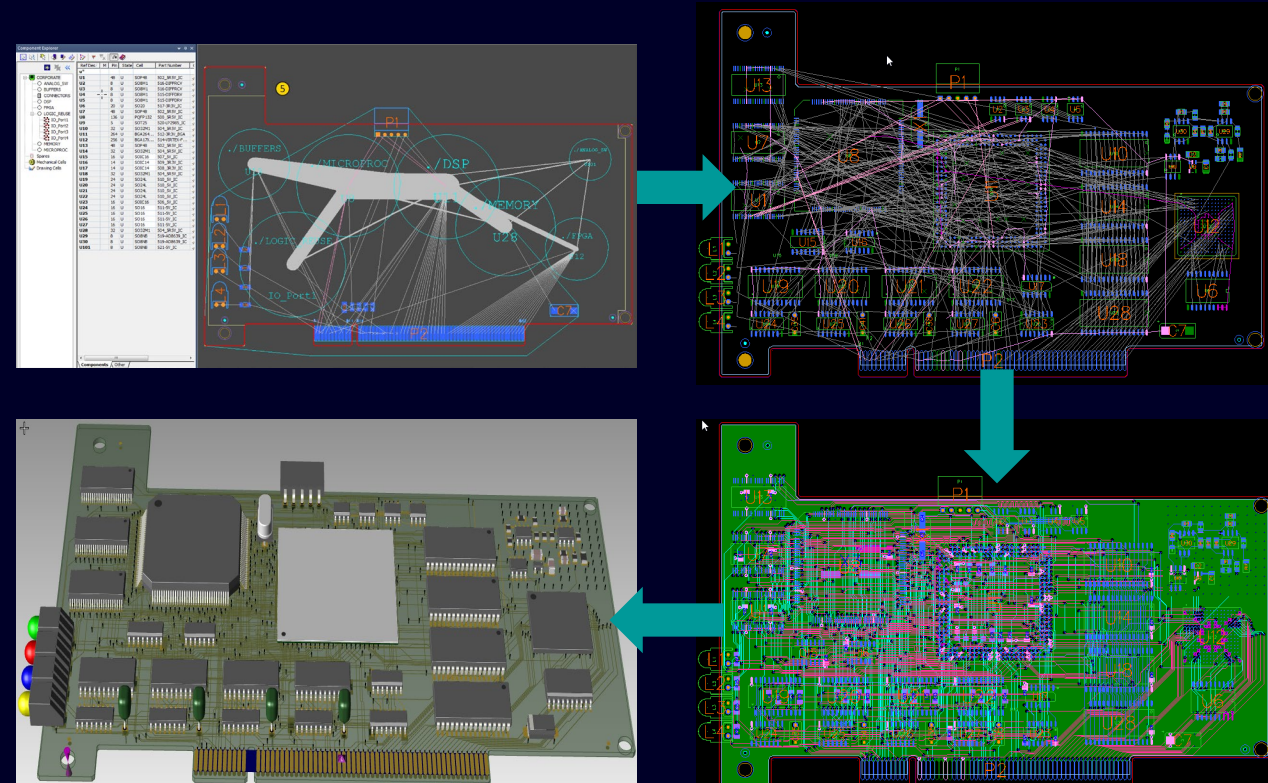
Legacy methodologies can't meet today's design complexities

Roadblocks!

- Unfamiliar with automated functions in tool
- Feeling of less control of design, don't trust
- Legacy practices are the standard

Best Practice

- Assign parts to groups/clusters
- Route using a combination of interactive and automated routing
- Generate outputs utilizing built-in automation functionality



Analog/Digital/RF Co-design

Problem!

RF circuits are not optimally integrated into the design

Roadblocks!

- Disparate disciplines working in isolation
- Outsource to specialist or SME
- Siloed organizations/specialists

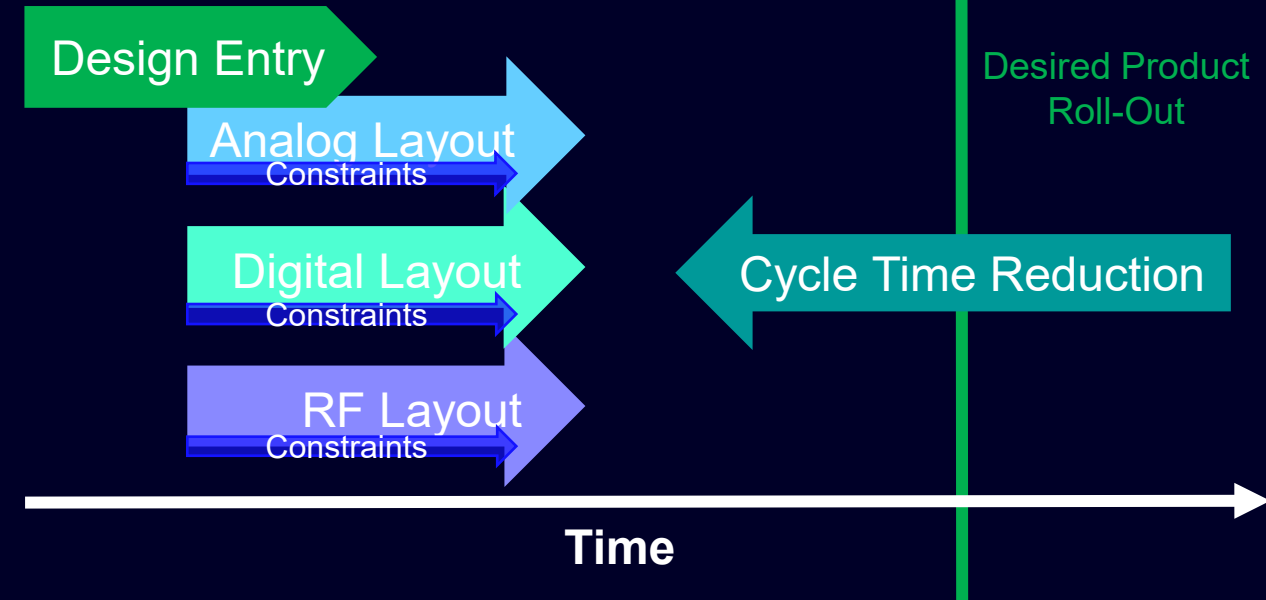
Best Practice

- Implement co-design and integration between Analog/Digital/RF engineers
- Integrate RF circuitry concurrently in design
- Adopt latest exchange formats

Traditional Serial Design Layout



Simultaneous Design Layout



Concurrent Design – Schematic / Layout

Problem!

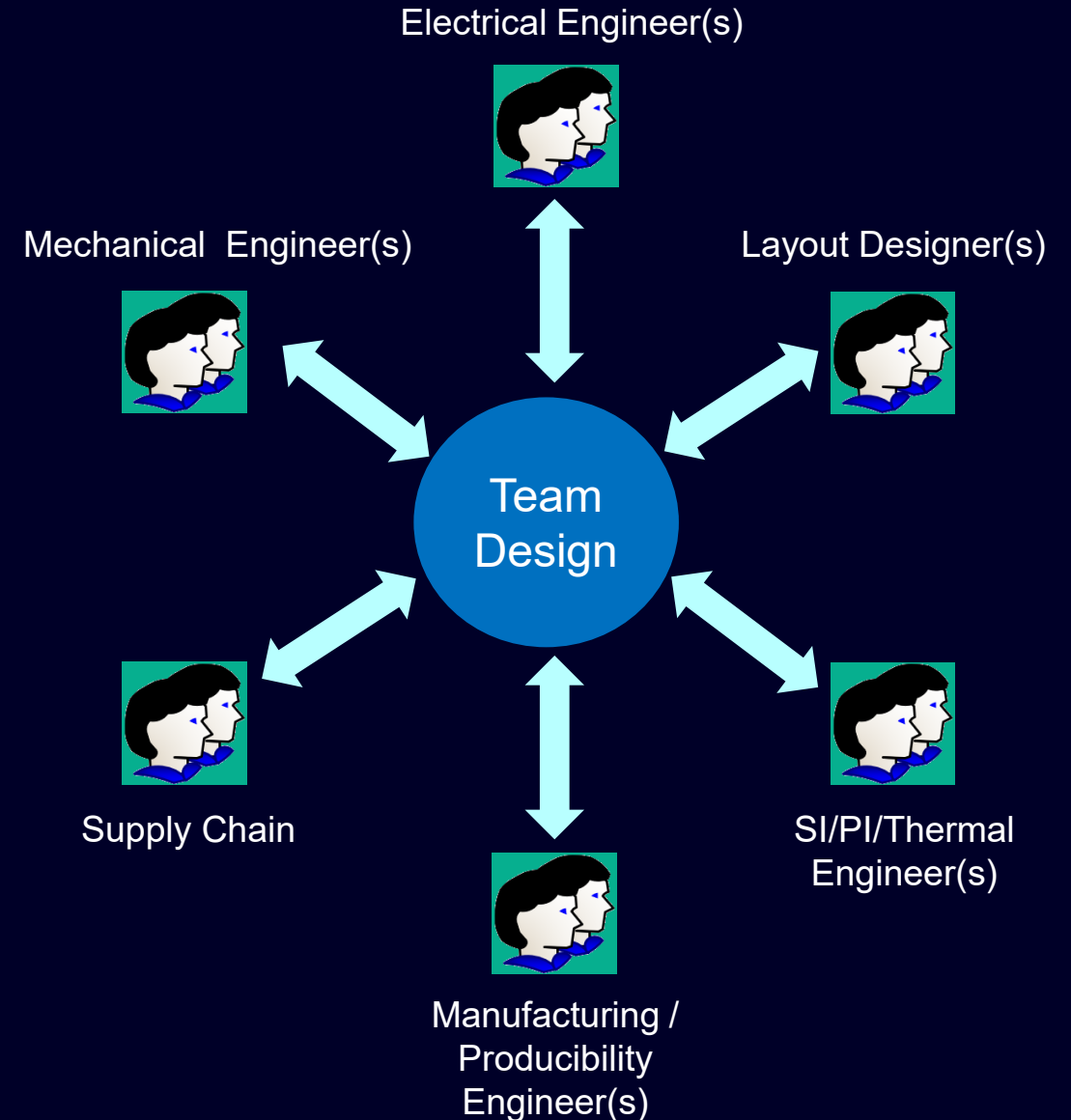
Legacy serial approach is inefficient

Roadblocks!

- Not wanting others to touch/modify their work
- Inefficient work distribution / working in silo's
- No incentive to change

Best Practice

- Utilize advanced capabilities - schematic/layout
- Optimize multidiscipline integration in database
- Optimize team utilization



Design Reuse

Problem!

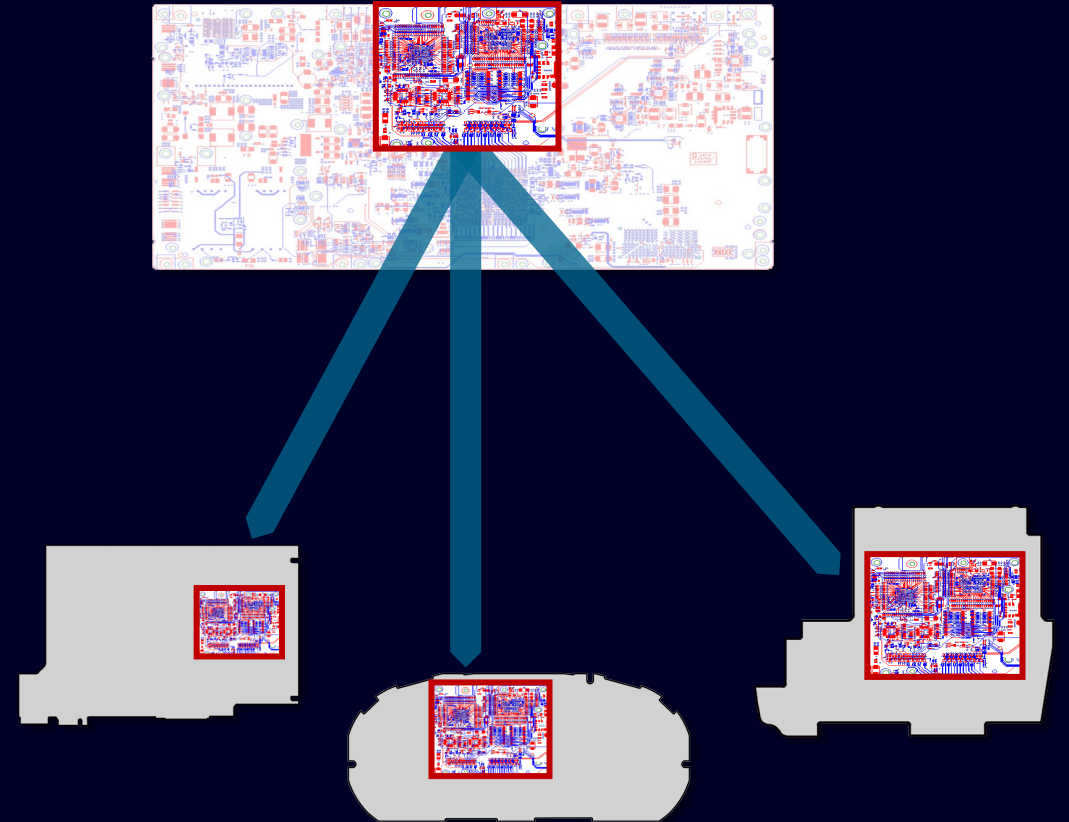
Re-inventing the wheel and poor enterprise utilization

Roadblocks!

- Inefficient process for sharing data
- Don't trust another engineer's circuit/layout
- No pressure to improve current methodology

Best Practice

- Utilize proven circuitry and layouts – lower risk
- Manage modules same as individual components
- Share validated HW IP throughout enterprise



Constraint Driven Design

Problem!

Inefficient implementation of design rules

Roadblocks!

- Too much overhead to setup/implement/maintain
- Takes too long to implement
- Not familiar/proficient with tool

Best Practice

- Establish constraint management process
- Utilize automation to control, meet, and verify requirements were implemented

Scheme/Net Class/Layer	Index	Type	Display Pattern	Via Assignments	Route	Trace Width	
						Minimum	Typical
(Master)							
(Default)			(None)	xxx (default)	<input checked="" type="checkbox"/>	4	
CLOCKS			(None)	xxx (default)	<input checked="" type="checkbox"/>	5	
DP_100_OHM			(None)	xxx (default)	<input checked="" type="checkbox"/>	4	
CLOCK2			(None)	xxx (default)	<input checked="" type="checkbox"/>	5	
PWR_020_MIL			(None)	xxx (default)	<input checked="" type="checkbox"/>	8	
BSYNC			(None)	xxx (default)	<input checked="" type="checkbox"/>	5	
FADDR			(None)	xxx (default)	<input checked="" type="checkbox"/>	5	
FDATA			(None)	xxx (default)	<input checked="" type="checkbox"/>	5	
(Minimum)							
(Default)						3	
CLOCKS						5	
DP_100_OHM						4	
CLOCK2						5	
PWR_020_MIL						8	
BSYNC						5	
FADDR						3	
FDATA						3	
FPGA							
(Default)				xxx (default)	<input checked="" type="checkbox"/>	3	
FADDR				xxx (default)	<input checked="" type="checkbox"/>	3	
CLOCKS				xxx (default)	<input checked="" type="checkbox"/>	5	
DP_100_OHM				xxx (default)	<input checked="" type="checkbox"/>	4	
CLOCK2				xxx (default)	<input checked="" type="checkbox"/>	5	
PWR_020_MIL				xxx (default)	<input checked="" type="checkbox"/>	8	
BSYNC				xxx (default)	<input checked="" type="checkbox"/>	5	
FDATA				xxx (default)	<input checked="" type="checkbox"/>	3	



Advanced Design – Rigid-flex

Problem!

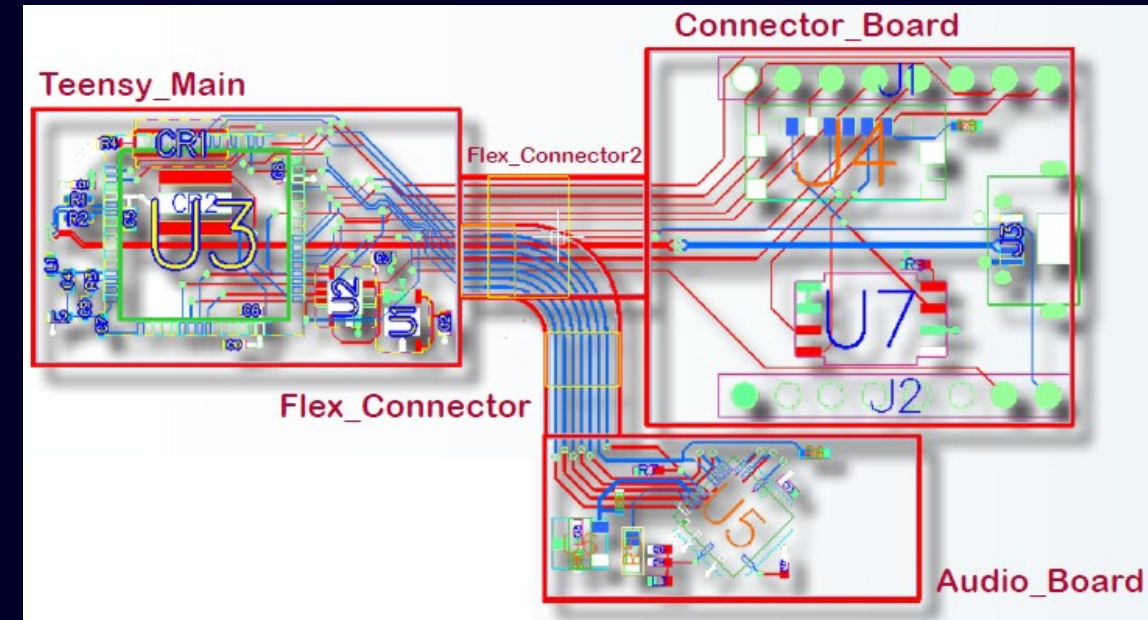
Rigid-flex design using rigid structures is inefficient and error prone

Roadblocks!

- Not familiar/proficient with tool and or subject
- Use standard rigid PCB approach for everything
- Requires specialist/SME

Best Practice

- Utilize updated rigid-flex design methodology to efficiently define board outlines, stack-ups, and regional constraints



Advanced Design – High Density Interconnect (HDI)

Problem!

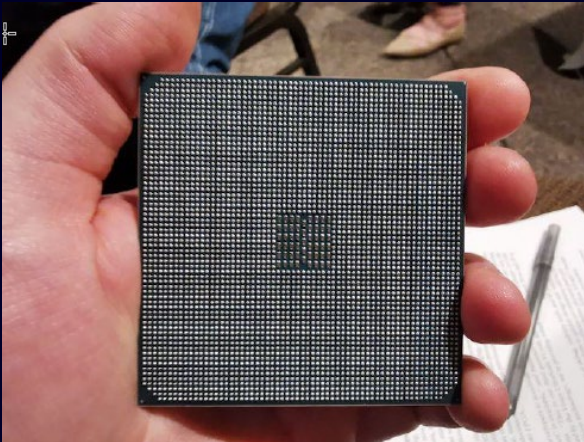
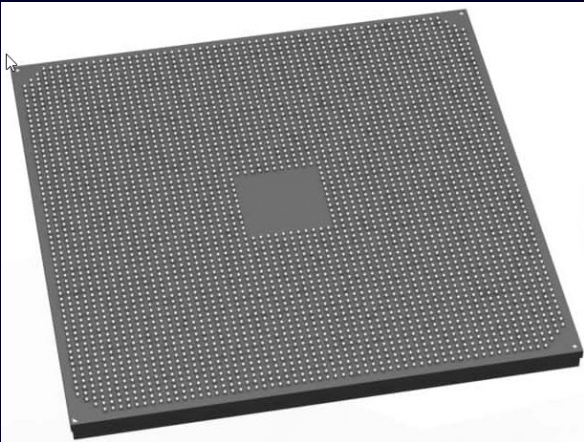
Implementing traditional via structures results in delays/cost

Roadblocks!

- Not familiar/proficient with tool and or subject
- Inefficient processes reduce opportunities to use HDI

Best Practice

- Capabilities are commonly available in most tools... stop doing work-arounds!

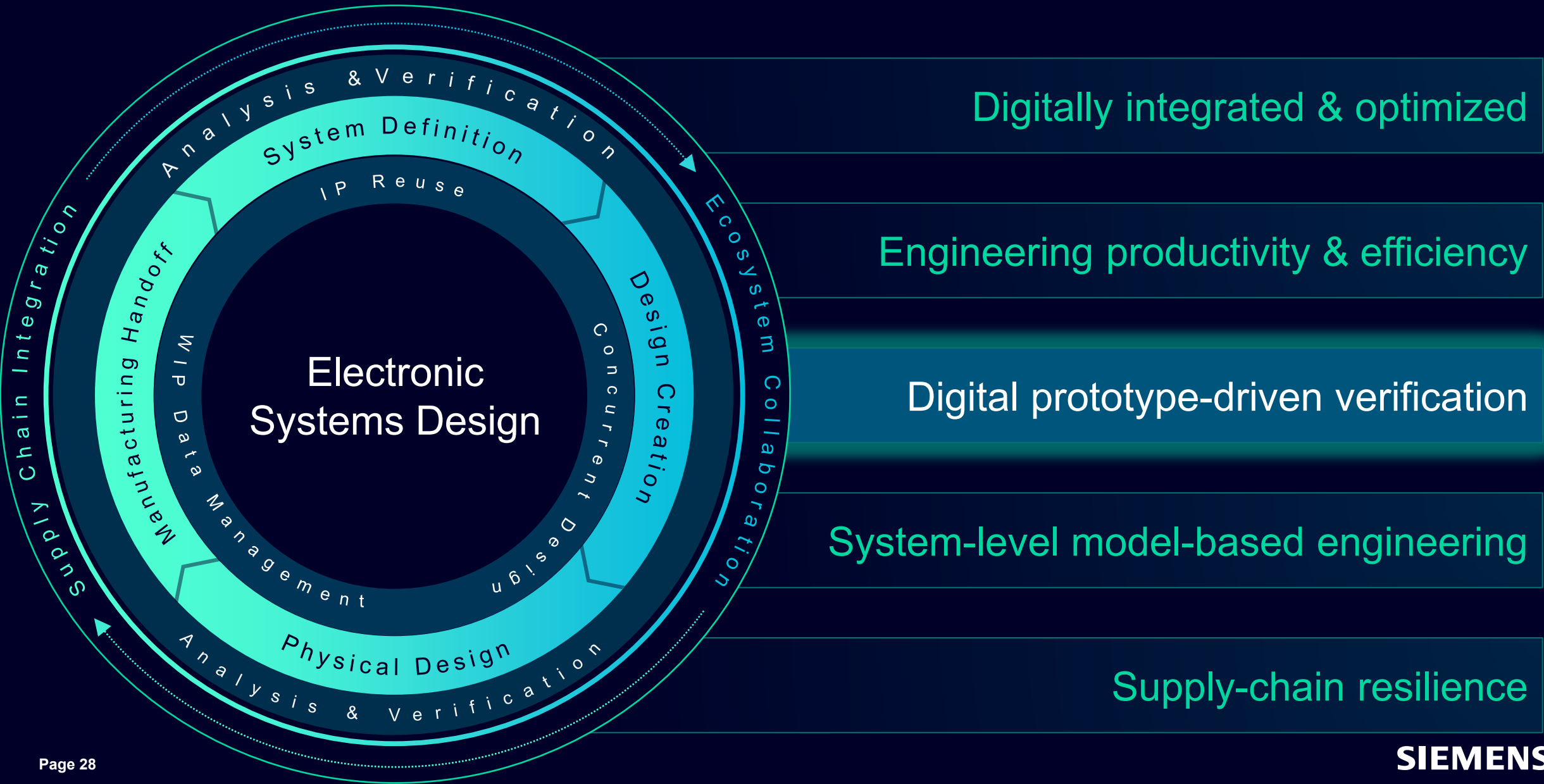


AMD Xilinx - IC FPGA VIRTEX-UP 3824FCBGA (65x65)

N Layers	A	B	C	D	E	F	G
	THRU-HOLE	HDI BLIND	HDI BL/BU	1BU BLIND	2BU BLIND	2BU BL.BU	2BU BL.BU
	N	1+N+1	1+bN+1	1+N+1	2+N+2	2+bN+2	2+bN+2
	blind via*	L1-L2	L1-L2	skip via L1-L3	staggered L1-L2, L2-L	skip via L1-L3	staggered L1-L2, L2-L
	buried via	none	L2-L(N-1)	L2-L(N-1)	none	L2-L(N-1)	L3-L(N-2)

Examples of HDI constructions types and methodologies

Pillars of Best Practices



Shift Left – Analysis (Part 1- Analysis)

Problem!

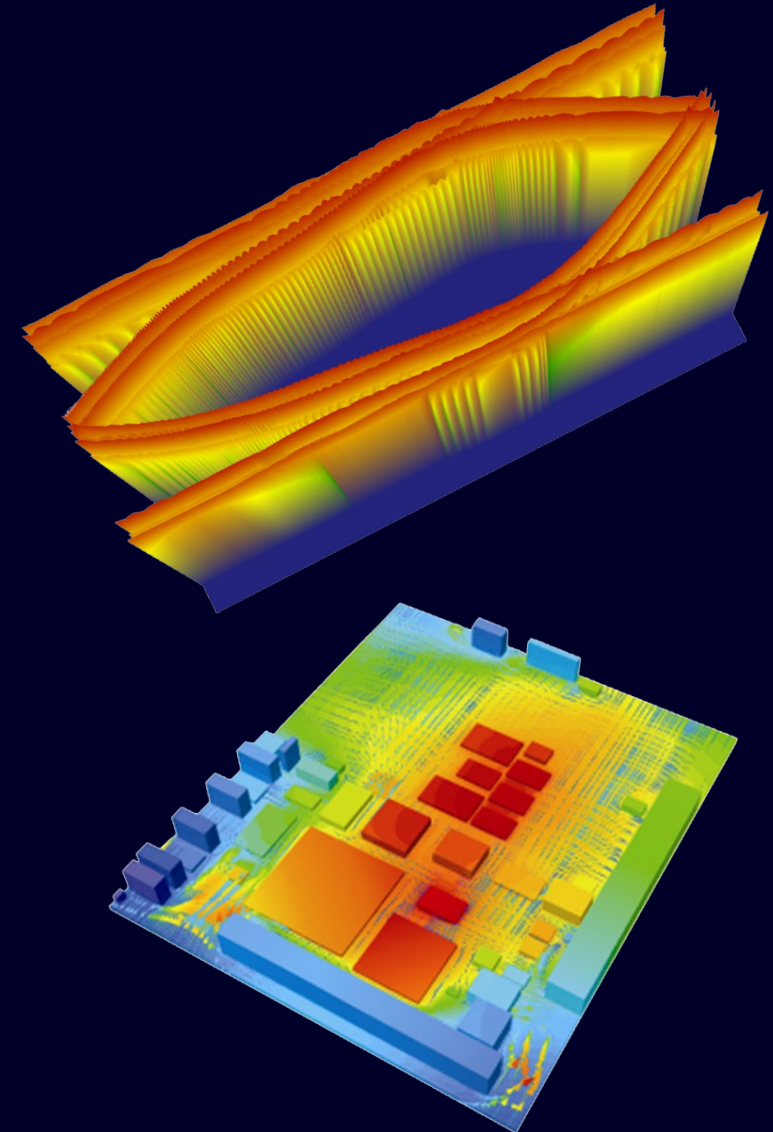
Re-spins are normalized due to analysis not being run

Roadblocks!

- Multiple re-spins already planned in schedule
 - "No time to complete analysis" mentality
 - Too much overhead to setup/implement/maintain
-

Best Practice

- Account for analysis in the initial project schedule
- Don't eliminate analysis in trying to reduce project schedule and cost
- Shift left multidiscipline analyses of Schematic, Thermal, SI/PI, AMS, DFM, Specialist/Design Author, HASS/HALT, DFT to eliminate errors



Shift Left – Analysis (Part 2 – Domain Specialist)

Problem!

Domain specialists working in silos and too far downstream

Roadblocks!

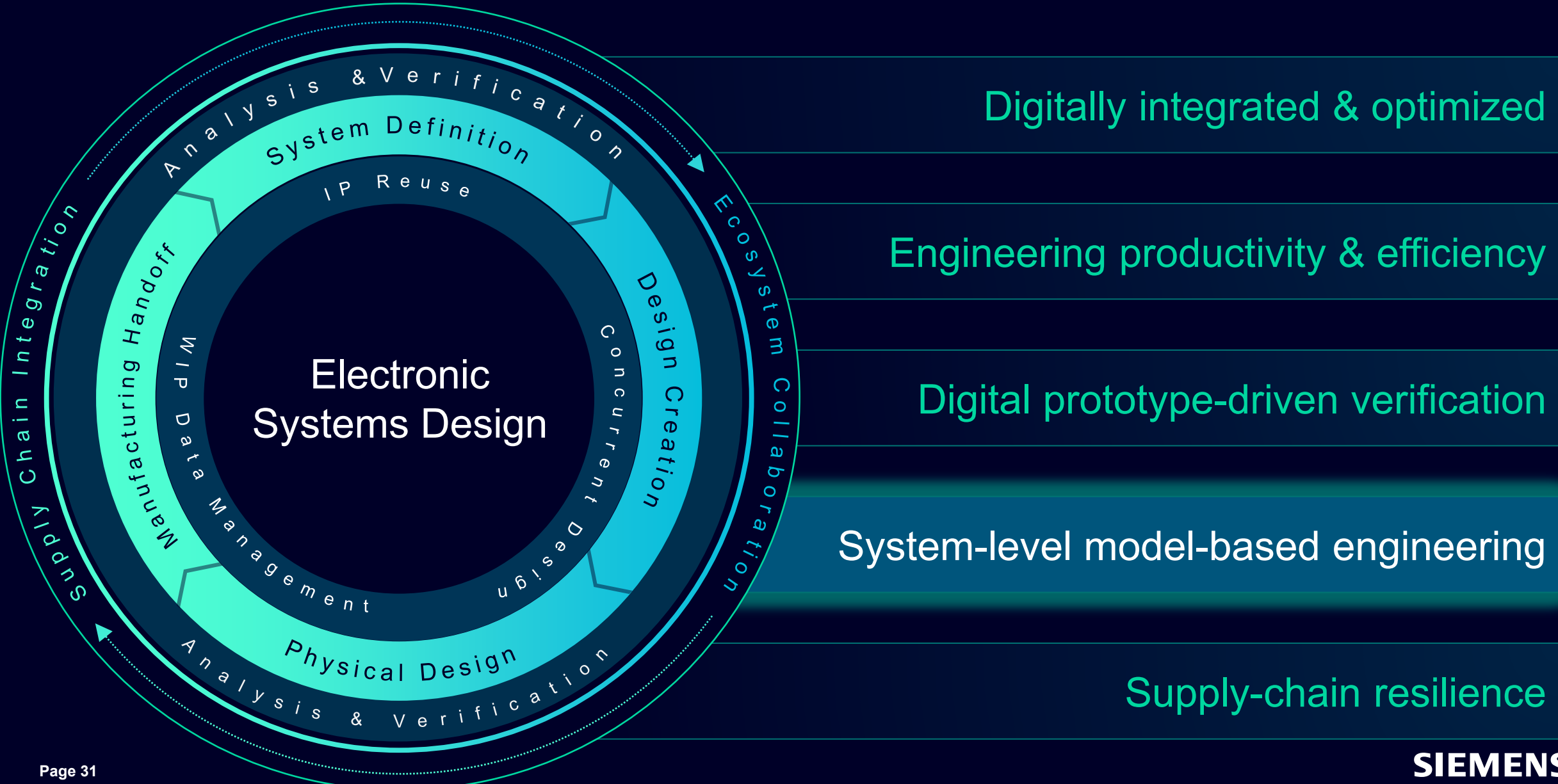
- No domain specialist available
- Design process not optimized for analysis
- "That's not my job" mentality

Best Practice

- Optimize multi-domain collaboration/integration
- Utilize domain specialist earlier in the process
- Utilize today's advanced capabilities within tools
- Cross-train skillset (remove single source)



Pillars of Best Practices



Multi-board Design

Problem!

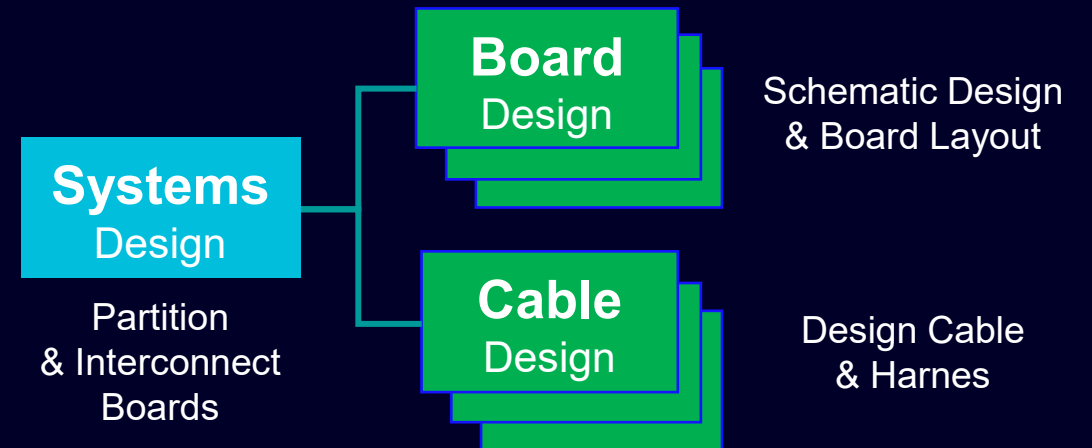
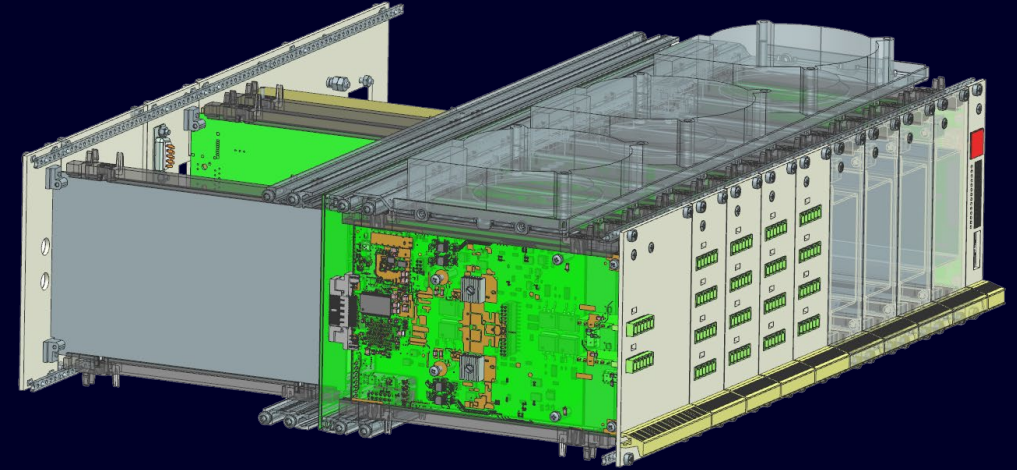
Full systems design done in a vacuum, and by siloed team members

Roadblocks!

- Not familiar/proficient with tool
- Too much overhead to setup/implement/maintain
- Too expensive to implement

Best Practice

- Implement multi-board model-based engineering for cross-system optimization options (size / performance)
- Remove siloed engineering approach



FPGA/PCB Optimization

Problem!

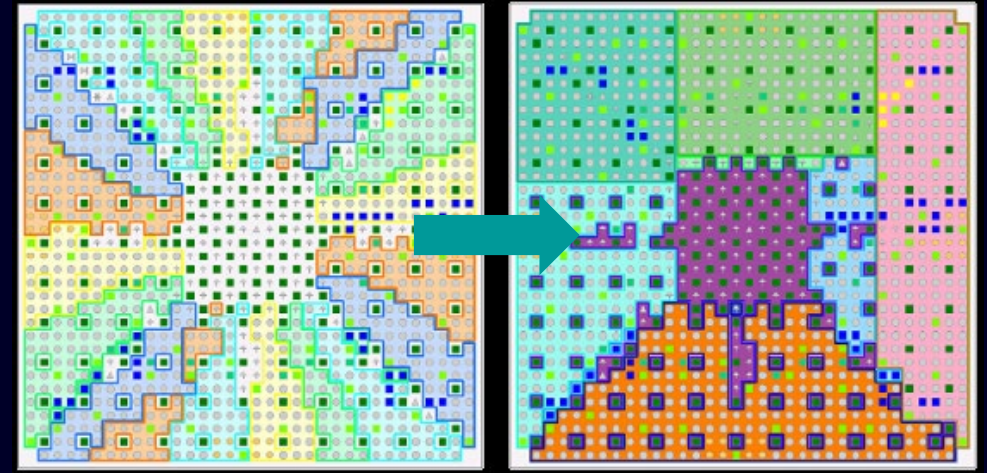
FPGA design methodology is inefficient in its ability to optimize FPGA pin-out configurations

Roadblocks!

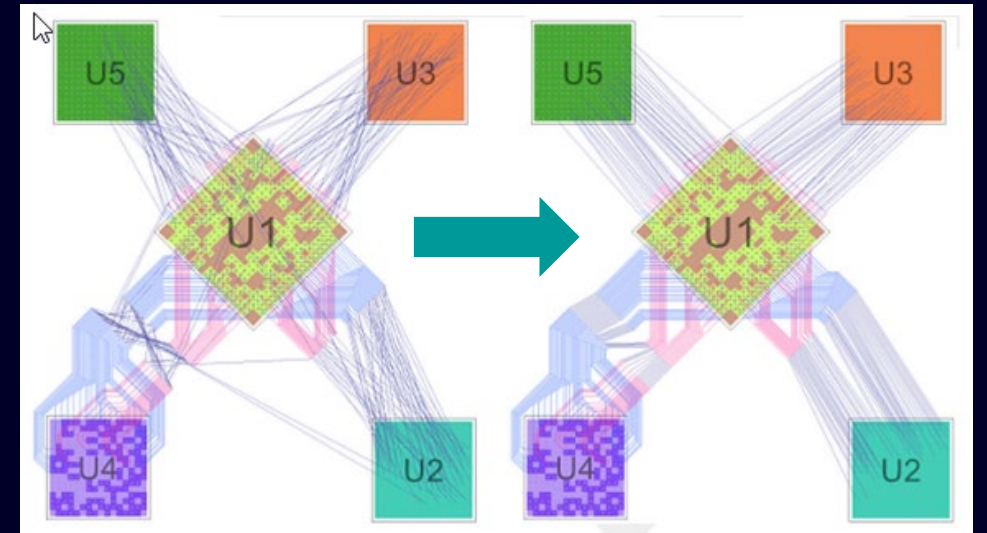
- Too much overhead to setup/implement/maintain
- FPGA tools good enough (even if they don't consider layout)

Best Practice

- Utilize FPGA/PCB integration
- Configure FPGA pin-out for routing optimization
- Enable efficient FPGA pin-swapping capability



Ten banks partitioned into seven custom pins groups



Connectivity needs to be optimized across multiple devices

IC/Package/PCB

Problem!

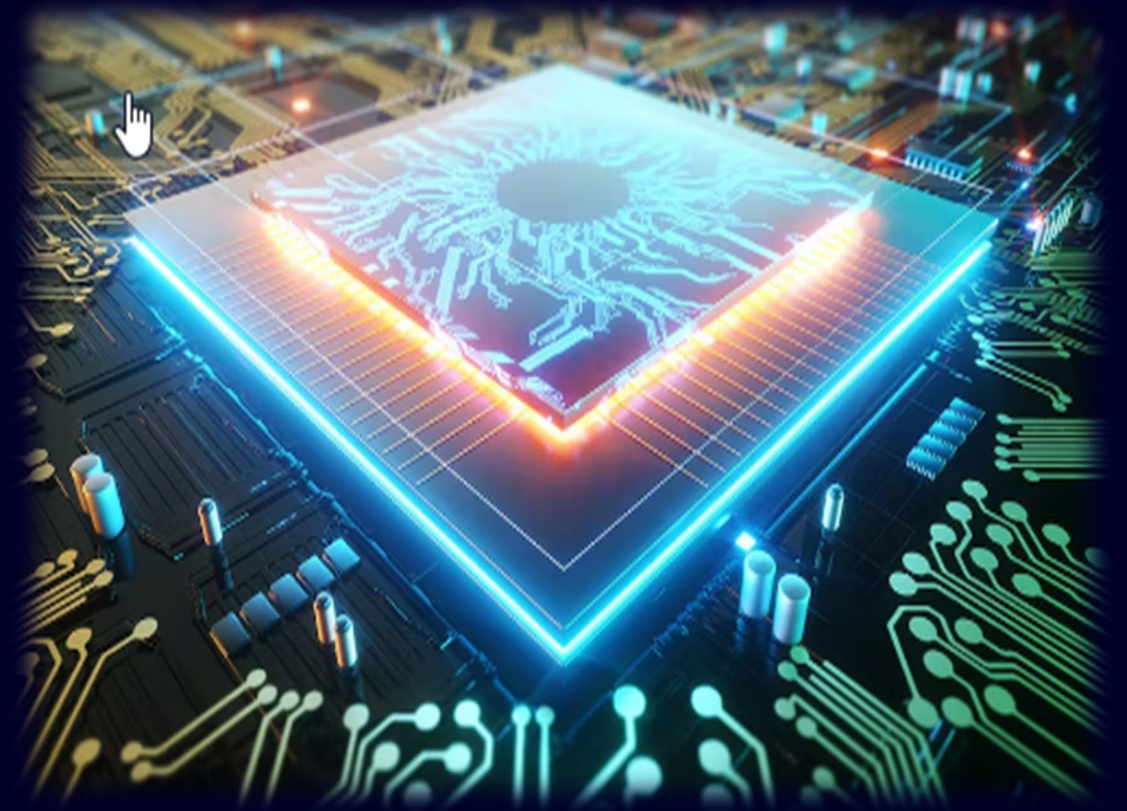
Inefficient IC/package/PCB optimization, not considering all "fabrics" simultaneously

Roadblocks!

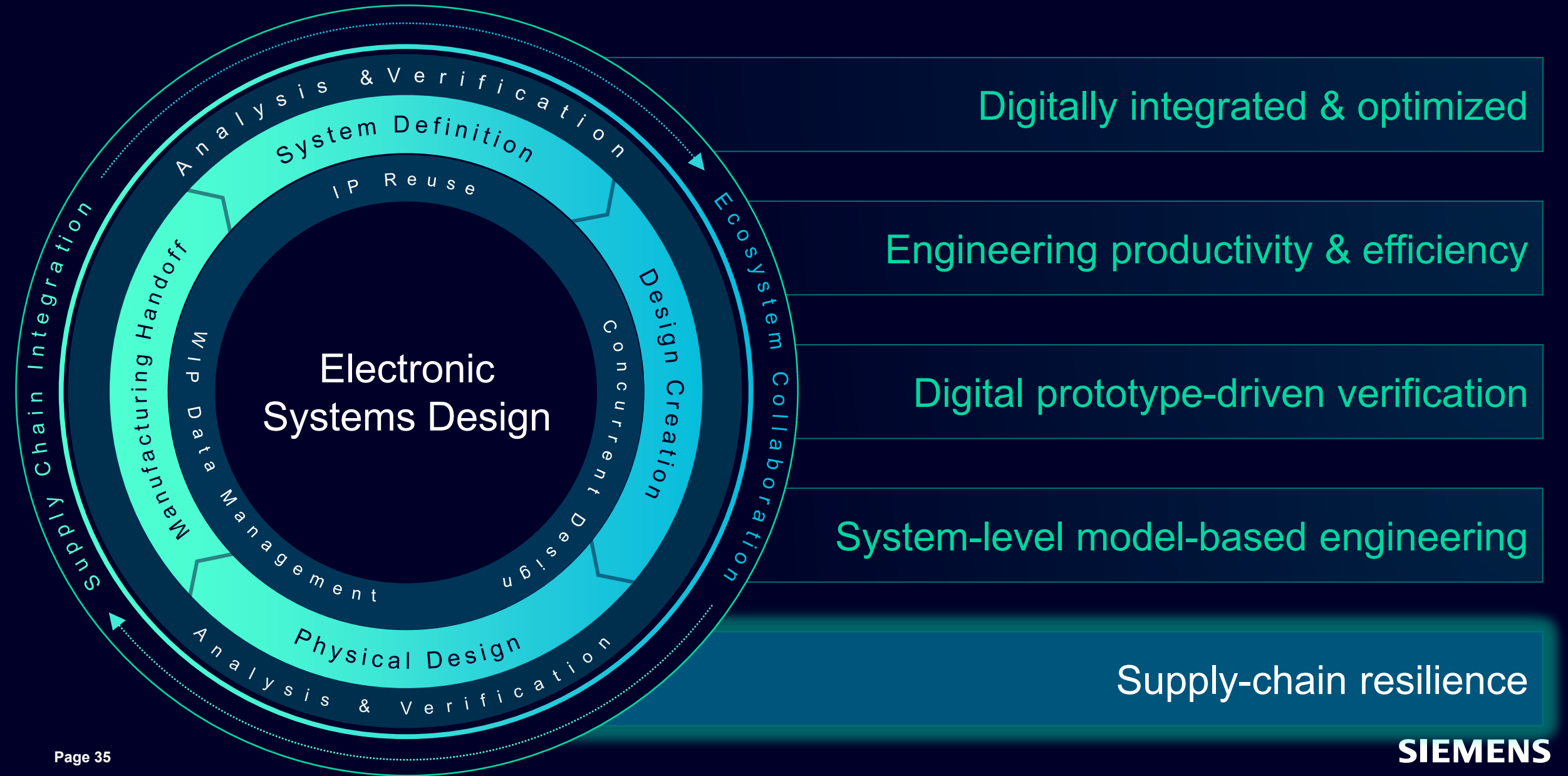
- Not familiar/proficient with tool
- Too much overhead to setup/implement/maintain
- Too expensive to implement

Best Practice

- Utilize Systems-Level Model Based Engineering
- Optimize the system IO
- Enable digital twin



Pillars of Best Practices



Supply-Chain Resilience

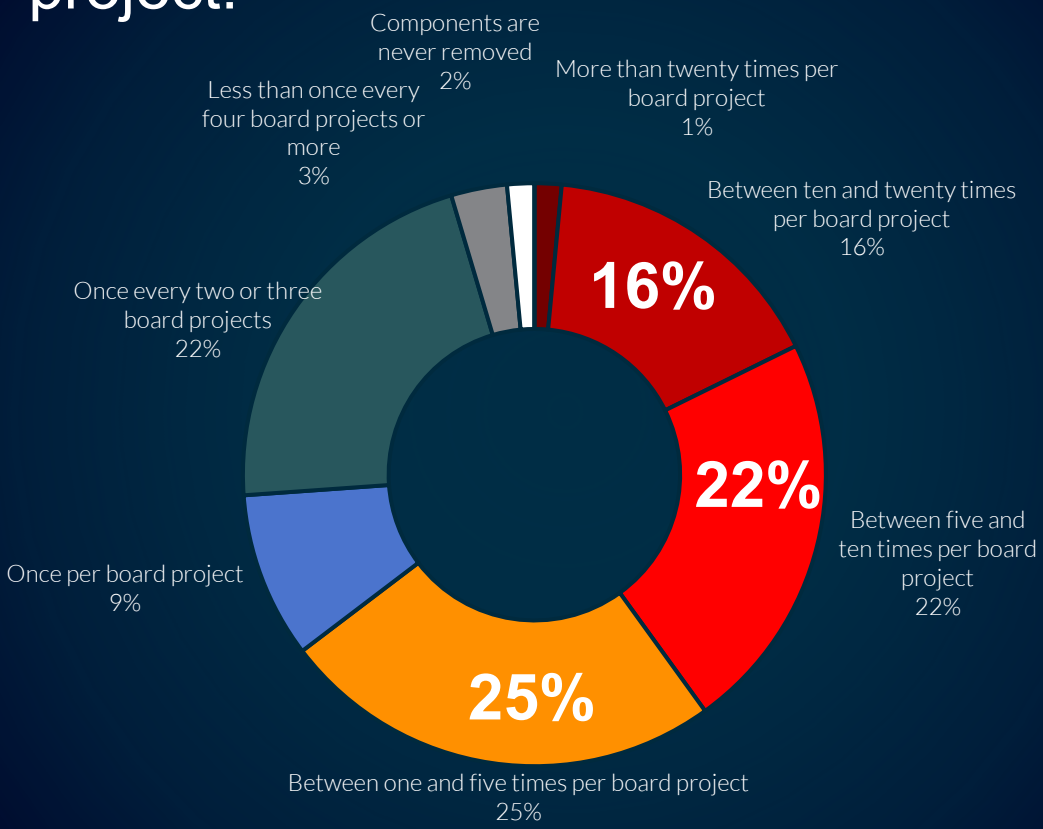


The only abundance seen lately in the electronic components market is the quantity of calendar pages marking how long the supply shortage has lasted...the shortage has no clear end in sight, as the market continues to navigate a perfect storm of high demand and short supply for electronic products.

Jabil

- ✓ Integrated sourcing an engineering collaboration bringing supply-chain information into the engineer's desktop
- ✓ Accurate & up-to-date component information available in enterprise libraries
- ✓ Early sourcing optimization decision with direct BoM integration

39% are removing components between five to twenty times per PCB project!



The average number of times engineers must remove an electronic component from their board design due to availability, lifecycle, or compliance.

Source: Lifecycle Insights April 2022



Design for Resilience

Problem!

Siloed teams, legacy processes and ineffective risk management

Roadblocks!

- Just-in-time approach current mode of operation
- Not sure how to address supply chain issues
- Too much overhead to setup/implement/maintain

Best Practice

- Implement outside-in approach with supply-chain intelligence by shifting left best-known part availability, BOM validation, and validation of alternates at point of design
- Remove barriers from siloed teams and optimize operations and communications



Image: Inefficient Mapping by Linda Knight

Summary

Best Practices

- Understand the decisions made upstream and their effects downstream
- Utilize today's EDA tool automation and horsepower to your advantage
- Be open to new methodologies
- Know that company culture can be the ultimate roadblock
- Design for resilience



| Thank You!

Stephen V. Chavez

MIT, CID+, CPCD

Sr Product Marketing Manager – Siemens

Chairman – Printed Circuit Engineering Association (PCEA)